WHAT IS CLAIMED IS:

1. A method to suppress a short channel effect of a semiconductor device, comprising:

forming a gate structure on a substrate;

forming a source/drain extension region and a source/drain region in the substrate beside the gate structure;

performing a pocket ion implantation process to form a pocket doped region under the source/drain extension region; and

performing a rapid thermal process to anneal the source/drain extension region, the source/drain region and the pocket doped region concurrently.

2. The method of claim 1, wherein the source/drain extension region and the source/drain region are implanted with an N-type dopant.

3. The method of claim 2, wherein the N-type dopant is selected from the group consisting of antimony ions and arsenic ions.

4. The method of claim 2, wherein an implantation energy for forming the source/drain extension region is about 10 KeV.

5. The method of claim 2, wherein a dosage that is implanted for the source/drain extension region is about $3x10^{14}/cm^2$.

6. The method of claim 1, wherein the pocket doped region is doped with a p-type doapnt.

7. The method of claim 6, wherein the p-type dopant includes indium ions.

8. The method of claim 7, wherein an implantation energy for the pocket doped implantation process is about 60 keV.

9. The method of claim 7, wherein a dosage of the pocket doped implantation process is about $1x10^{13}/cm^2$.

10. The method of claim 7, wherein the pocket doped implantation tilt angle is about 30 degrees.

11. The method of claim 1, wherein the rapid thermal process is conducted under a temperature of about 900 degrees Celsius for about 10 seconds.

12. A method to suppress a short channel effect of a semiconductor device, comprising:

forming a gate structure on a substrate;

performing a first ion implantation process to form a source/drain extension region in the substrate using the gate structure as an implantation mask;

forming a spacer on a sidewall of the gate structure;

performing a second ion implantation process to form a source/drain region using the spacer as an implantation mask;

performing a pocket doped implantation process to form a pocket doped region under the source/drain extension region after the formation of the source/drain extension region and the source/drain region; and

performing a rapid thermal process after the formation of the pocket doped region to anneal the source/drain extension region, the source/drain region and the pocket doped region.

13. The method of claim 12, wherein a dopant implanted for the source/drain extension region and the source/drain region is selected from the group consisting of antimony ions and arsenic ions.

14. The method of claim 12, wherein an implantation energy for the first ion implantation process is about 10 KeV.

15. The method of claim 12, wherein a dosage of the first ion implantation process is about $3x10^{14}/cm^2$.

16. The method of claim 12, wherein a dopant implanted for the pocket doped region includes indium ions.

17. The method of claim 16, wherein an implantation energy for the pocket doped implantation is about 60 keV.

18. The method of claim 16, wherein a dosage of the pocket doped implantation process is about $1x10^{13}/cm^2$.

19. The method of claim 16, wherein the pocket doped implantation is conducted at a tilt angle of about 30 degrees.

20. The method of claim 12, wherein the rapid thermal process is conducted under a temperature of about 900 degrees Celsius for about 10 seconds.